

DM7476

Dual Master-Slave J-K Flip-Flops with Clear, Preset, and Complementary Outputs

General Description

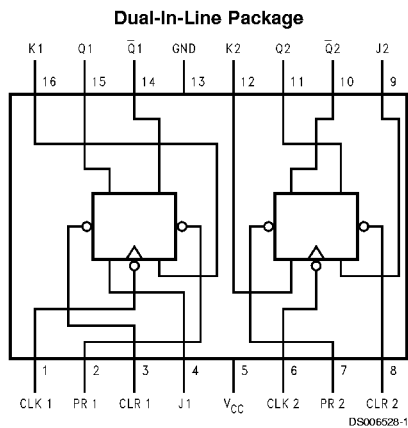
This device contains two independent positive pulse triggered J-K flip-flops with complementary outputs. The J and K data is processed by the flip-flop after a complete clock pulse. While the clock is low the slave is isolated from the master. On the positive transition of the clock, the data from the J and K inputs is transferred to the master. While the clock is high the J and K inputs are disabled. On the negative transition of the clock, the data from the master is transferred to the slave. The logic state of J and K inputs must not be al-

lowed to change while the clock is high. The data is transferred to the outputs on the falling edge of the clock pulse. A low logic level on the preset or clear inputs will set or reset the outputs regardless of the logic levels of the other inputs.

Features

- Alternate Military/Aerospace device (5476) is available. Contact a Fairchild Semiconductor Sales Office/Distributor for specifications.

Connection Diagram



Order Number 5476DMQB, 5476FMQB,
DM5476J, DM5476W or DM7476N
See Package Number J16A, N16E or W16A

Function Table

Inputs					Outputs	
PR	CLR	CLK	J	K	Q	\bar{Q}
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H	H
H	H	\neg	L	L	Q ₀	\bar{Q}_0
H	H	\neg	H	L	H	L
H	H	\neg	L	H	L	H
H	H	\neg	H	H	Toggle	

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level
 \neg = Positive pulse data. The J and K inputs must be held constant while the clock is high. Data is transferred to the outputs on the falling edge of the clock pulse.
Q₀ = The output logic level before the indicated input conditions were established.
Toggle = Each output changes to the complement of its previous level on each complete active high level clock pulse.
Note 1: This configuration is nonstable; that is, it will not persist when the preset and/or clear inputs return to their inactive (high) level.

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