

# SN5475, SN5477, SN54LS75, SN54LS77 SN7475, SN74LS75 4-BIT BISTABLE LATCHES

SDLS120 – MARCH 1974 – REVISED MARCH 1988

**FUNCTION TABLE**  
(each latch)

INPUTS		OUTPUTS	
D	C	Q	$\bar{Q}$
L	H	L	H
H	H	H	L
X	L	$Q_0$	$\bar{Q}_0$

H = high level, L = low level, X = irrelevant  
 $Q_0$  = the level of Q before the high-to-low transition of G

## description

These latches are ideally suited for use as temporary storage for binary information between processing units and input/output or indicator units. Information present at a data (D) input is transferred to the Q output when the enable (C) is high and the Q output will follow the data input as long as the enable remains high. When the enable goes low, the information (that was present at the data input at the time the transition occurred) is retained at the Q output until the enable is permitted to go high.

The '75 and 'LS75 feature complementary Q and  $\bar{Q}$  outputs from a 4-bit latch, and are available in various 16-pin packages. For higher component density applications, the '77 and 'LS77 4-bit latches are available in 14-pin flat packages.

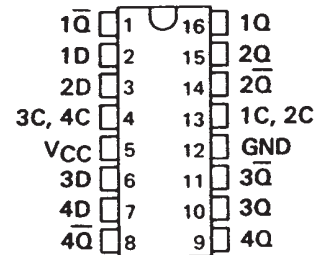
These circuits are completely compatible with all popular TTL families. All inputs are diode-clamped to minimize transmission-line effects and simplify system design. Series 54 and 54LS devices are characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ ; Series 74, and 74LS devices are characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

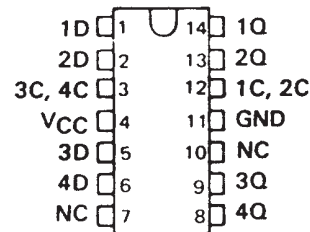
Supply voltage, $V_{CC}$ (See Note 1)	7 V
Input voltage: '75, '77	5.5 V
'LS75, 'LS77	7 V
Interemitter voltage (see Note 2)	5.5 V
Operating free-air temperature range: SN54'	$-55^{\circ}\text{C}$ to $125^{\circ}\text{C}$
SN74'	$0^{\circ}\text{C}$ to $70^{\circ}\text{C}$
Storage temperature range	$-65^{\circ}\text{C}$ to $150^{\circ}\text{C}$

NOTES: 1. Voltage values are with respect to network ground terminal.  
 2. This is the voltage between two emitters of a multiple-emitter input transistor and is not applicable to the 'LS75 and 'LS77.

**SN5475, SN54LS75 . . . J OR W PACKAGE**  
**SN7475 . . . N PACKAGE**  
**SN74LS75 . . . D OR N PACKAGE**  
 (TOP VIEW)

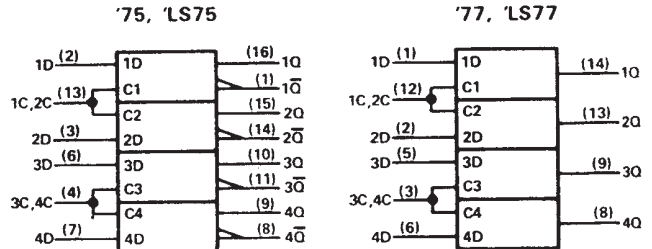


**SN5477, SN54LS77 . . . W PACKAGE**  
 (TOP VIEW)



NC - No internal connection

## logic symbols†



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.