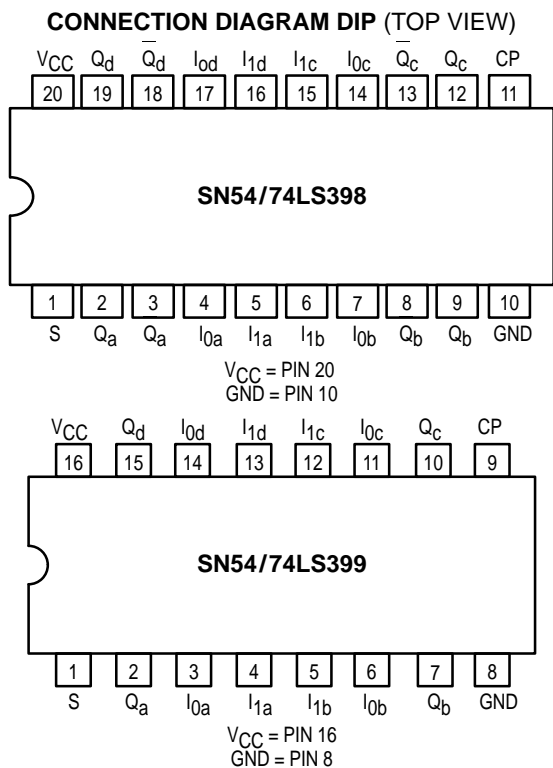




QUAD 2-PORT REGISTER

The SN54/74LS398 and SN54/74LS399 are Quad 2-Port Registers. They are the logical equivalent of a quad 2-input multiplexer followed by a quad 4-bit edge-triggered register. A Common Select input selects between two 4-bit input ports (data sources). The selected data is transferred to the output register on the LOW-to-HIGH transition of the Clock input. The SN54/74LS398 features both Q and Q outputs, while the SN54/74LS399 has only Q outputs.

- Select From Two Data Sources
- Fully Positive Edge-Triggered Operation
- Both True and Complemented Outputs on SN54/74LS398
- Input Clamp Diodes Limit High-Speed Termination Effects



PIN NAMES

S	Common Select Input
CP	Clock (Active HIGH Going Edge) Input
$I_{0a}-I_{0d}$	Data Inputs From Source 0
$I_{1a}-I_{1d}$	Data Inputs From Source 1
Q_a-Q_d	Register True Outputs (Note b)
Q_a-Q_d	Register Complementary Outputs (Note b)

LOADING (Note a)

	HIGH	LOW
S	0.5 U.L.	0.25 U.L.
CP	0.5 U.L.	0.25 U.L.
$I_{0a}-I_{0d}$	0.5 U.L.	0.25 U.L.
$I_{1a}-I_{1d}$	0.5 U.L.	0.25 U.L.
Q_a-Q_d	10 U.L.	5 (2.5) U.L.
Q_a-Q_d	10 U.L.	5 (2.5) U.L.

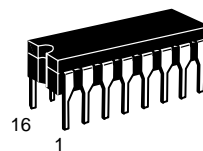
NOTES:

- a) 1 TTL Unit Load (U.L.) = 40 μ A HIGH/1.6 mA LOW.
 b) The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

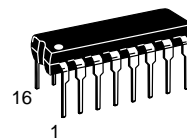
SN54/74LS398 SN54/74LS399

QUAD 2-PORT REGISTER

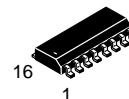
LOW POWER SCHOTTKY



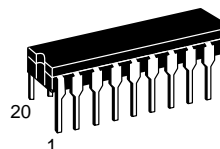
J SUFFIX
CERAMIC
CASE 620-09



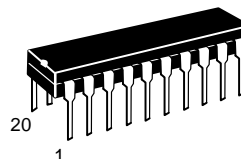
N SUFFIX
PLASTIC
CASE 648-08



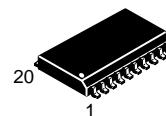
D SUFFIX
SOIC
CASE 751B-03



J SUFFIX
CERAMIC
CASE 732-03



N SUFFIX
PLASTIC
CASE 738-03



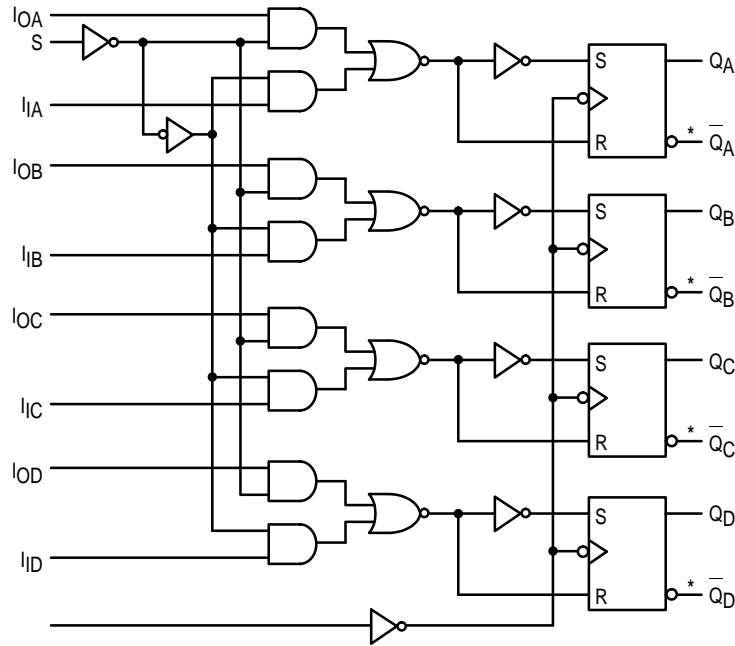
DW SUFFIX
SOIC
CASE 751D-03

ORDERING INFORMATION

SN54LSXXXJ	Ceramic
SN74LSXXXN	Plastic
SN74LSXXXDW	SOIC
SN74LSXXXD	SOIC

SN54/74LS398 • SN54/74LS399

FUNCTIONAL BLOCK DIAGRAM



* SN54/74LS398 only

FUNCTIONAL DESCRIPTION

The SN54/74LS398 and SN54/74LS399 are high-speed Quad 2-Port Registers. They select four bits of data from two sources (Ports) under the control of a common Select Input (S). The selected data is transferred to a 4-Bit Output Register synchronous with the LOW-to-HIGH transition of the Clock in-

put (CP). The 4-Bit RS type output register is fully edge-triggered. The Data inputs (I) and Select inputs (S) must be stable only a setup time prior to and hold time after the LOW-to-HIGH transition of the Clock input for predictable operation. The SN54/74LS398 has both Q and \bar{Q} Outputs available.

FUNCTION TABLE

INPUTS			OUTPUTS	
S	I ₀	I ₁	Q	Q*
l	l	X	L	H
l	h	X	H	L
h	X	l	L	H
h	X	h	H	L

*SN54/74LS398 only

l = LOW Voltage Level one setup time prior to the LOW-to-HIGH clock transition
h = HIGH Voltage Level one setup time prior to the LOW-to-HIGH clock transition
L = LOW Voltage Level
H = HIGH Voltage Level
X = Immaterial