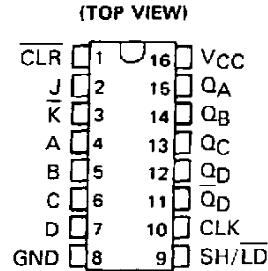


**SN54195, SN54LS195A, SN54S195,
SN74195, SN74LS195A, SN74S195**
4-BIT PARALLEL-ACCESS SHIFT REGISTERS
MARCH 1974—REVISED MARCH 1988

- Synchronous Parallel Load
- Positive-Edge-Triggered Clocking
- Parallel Inputs and Outputs from Each Flip-Flop
- Direct Overriding Clear
- J and \bar{K} Inputs to First Stage
- Complementary Outputs from Last Stage
- For Use in High Performance: Accumulators/Processors Serial-to-Parallel, Parallel-to-Serial Converters

SN54195, SN54LS195A, SN54S195 . . . J OR W PACKAGE
SN74195 . . . N PACKAGE
SN74LS195A, SN74S195 . . . D OR N PACKAGE



description

These 4-bit registers feature parallel inputs, parallel outputs, J- \bar{K} serial inputs, shift/load (SH/ \bar{LD}) control input, and a direct overriding clear. All inputs are buffered to lower the input drive requirements. The register has two modes of operation:

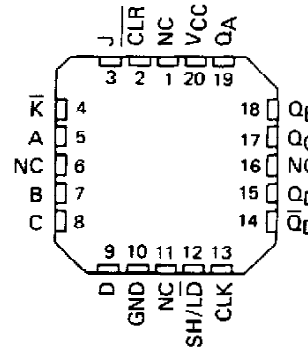
Parallel (broadside) load
Shift (in the direction Q_A toward Q_D)

Parallel loading is accomplished by applying the four bits of data and taking SH/ \bar{LD} low. The data is loaded into the associated flip-flop and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shifting is accomplished synchronously when SH/ \bar{LD} is high. Serial data for this mode is entered at the J- \bar{K} inputs. These inputs permit the first stage to perform as a J- \bar{K} , D-, or T-type flip-flop as shown in the function table.

The high-performance 'S195, with a 105-megahertz typical maximum shift-frequency, is particularly attractive for very-high-speed data processing systems. In most cases existing systems can be upgraded merely by using this Schottky-clamped shift register.

SN54LS195, SN54S195 . . . FK PACKAGE
(TOP VIEW)



NC - No internal connection

TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY	TYPICAL POWER DISSIPATION
'195	39 MHz	195 mW
'LS195A	39 MHz	70 mW
'S195	105 MHz	350 mW

FUNCTION TABLE

CLEAR	SHIFT/ LOAD	CLOCK	INPUTS				OUTPUTS						
			SERIAL J	SERIAL \bar{K}	PARALLEL A	PARALLEL B	PARALLEL C	PARALLEL D	Q_A	Q_B	Q_C	Q_D	\bar{Q}_D
L	X	X	X	X	X	X	X	L	L	L	L	H	
H	L	↑	X	X	a	b	c	d	a	b	c	d	\bar{d}
H	H	L	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	\bar{Q}_{D0}	
H	H	↑	L	H	X	X	X	Q_{A0}	Q_{A0}	Q_{Bn}	Q_{Cn}	\bar{Q}_{Cn}	
H	H	↑	L	L	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}	\bar{Q}_{Cn}	
H	H	↑	H	H	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}	\bar{Q}_{Cn}	
H	H	↑	H	L	X	X	X	\bar{Q}_{An}	Q_{An}	Q_{Bn}	Q_{Cn}	\bar{Q}_{Cn}	

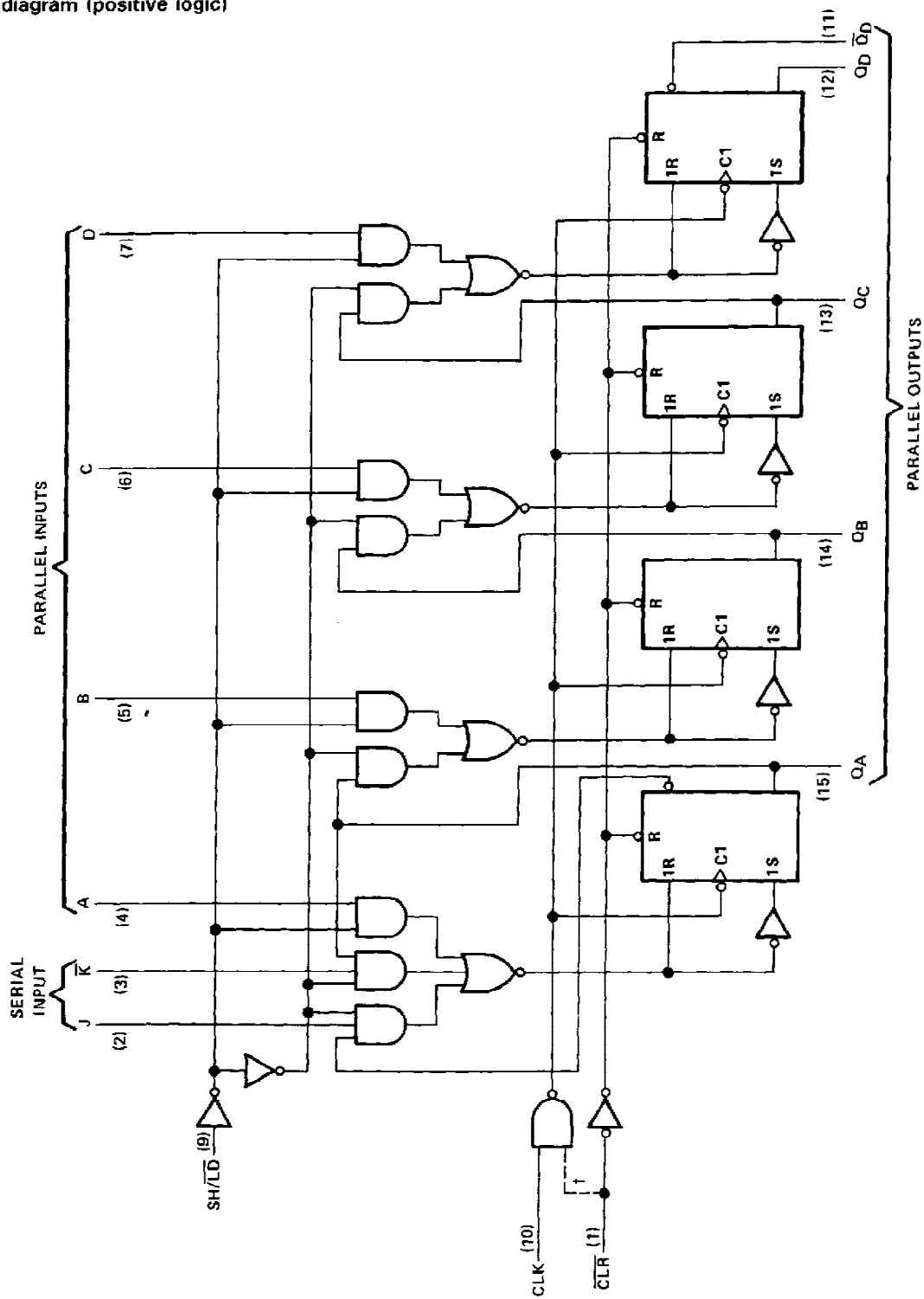
H = high level (steady state)
L = low level (steady state)
X = irrelevant (any input, including transitions)
↑ = transition from low to high level
a, b, c, d = the level of steady-state input at A, B, C, or D, respectively
 $Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0}$ = the level of Q_A, Q_B, Q_C , or Q_D , respectively, before the indicated steady-state input conditions were established
 Q_{An}, Q_{Bn}, Q_{Cn} = the level of Q_A, Q_B , or Q_C , respectively, before the most-recent transition of the clock

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



**SN54195, SN54LS195A, SN54S195,
SN74195, SN74LS195A, SN74S195
4-BIT PARALLEL-ACCESS SHIFT REGISTERS**

logic diagram (positive logic)



† This connection is made on '195 only.
Pin numbers shown are for D, J, N, and W packages.