

DM74174, DM74175 Hex/Quad D Flip-Flops with Clear

General Description

These positive-edge triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic. All have a direct clear input, and the quad (175) version features complementary outputs from each flip-flop.

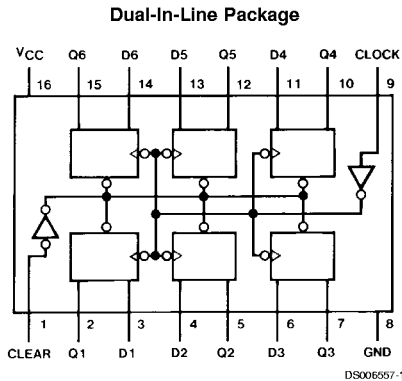
Information at the D inputs meeting the setup and hold time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

- 175 contains four flip-flops with double-rail outputs
- Buffered clock and direct clear inputs
- Individual data input to each flip-flop
- Applications include:
 - Buffer/storage registers
 - Shift registers
 - Pattern generators
- Typical clock frequency 40 MHz
- Typical power dissipation per flip-flop 38 mW
- Alternate Military/Aerospace device (54174, 54175) is available. Contact a Fairchild Semiconductor Sales Office/Distributor for specifications.

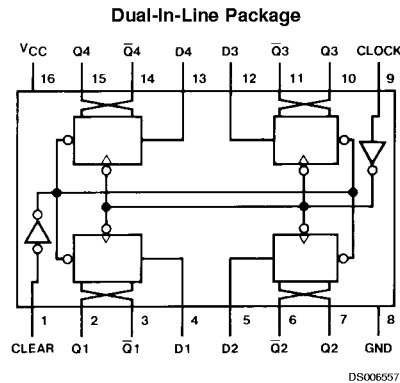
Features

- 174 contains six flip-flops with single-rail outputs

Connection Diagrams



Order Number 54174DMQB, 54174FMQB, DM54174J,
DM54174W or DM74174N
See Package Number J16A, N16E or W16A



Order Number 54175DMQB, 54175FMQB, DM54175J,
DM54175W or DM74175N
See Package Number J16A, N16E or W16A

Connection Diagrams (Continued)

Function Table

(Each Flip-Flop)

Inputs			Outputs	
Clear	Clock	D	Q	\bar{Q} (Note 1)
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	\bar{Q}_0

H = High Level (steady state)

L = Low Level (steady state)

X = Don't Care

↑ = Transition from low to high level

Q_0 = The level of Q before the indicated steady-state input conditions were established.

Note 1: 175 only