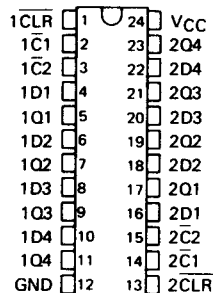


# SN54116, SN74116 DUAL 4-BIT LATCHES WITH CLEAR

DECEMBER 1972 - REVISED MARCH 1988

- Two Independent 4-Bit Latches in a Single Package
- Separate Clear Inputs Provide One-Step Clearing Operation
- Dual Gated Enable Inputs Simplify Cascading Register Implementations
- Compatible for Use with TTL Circuits
- Input Clamping Diodes Simplify System Design

SN54116 . . . J OR W PACKAGE  
SN74116 . . . N PACKAGE  
(TOP VIEW)



## description

These monolithic TTL circuits utilize D-type bistables to implement two independent four-bit latches in a single package. Each four-bit latch has an independent asynchronous clear input and a gated two-input enable circuit. When both enable inputs are low, the output levels will follow the data input levels. When either or both of the enable inputs are taken high, the outputs remain at the last levels setup at the inputs prior to the low-to-high-level transition at the enable input(s). After this, the data inputs are locked out.

The clear input is overriding and when taken low will reset all four outputs low regardless of the levels of the enable inputs.

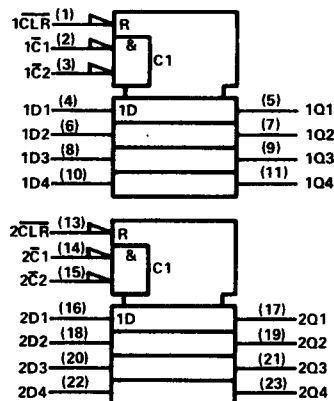
The SN54116 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ ; the SN74116 is characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

FUNCTION TABLE  
(EACH LATCH)

CLEAR	ENABLE		DATA	OUTPUT Q
	C1	C2		
H	L	L	L	L
H	L	L	H	H
H	X	H	X	$Q_0$
H	H	X	X	$Q_0$
L	X	X	X	L

H - high level, L - low level, X - irrelevant  
 $Q_0$  - the level of Q before these input conditions were established.

## logic symbol†



† This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

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TTL Devices

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