

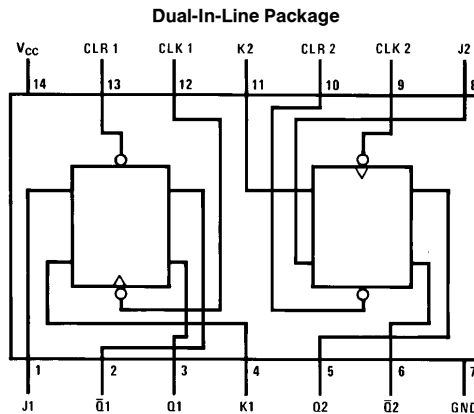
DM54LS107A/DM74LS107A Dual Negative-Edge-Triggered Master-Slave J-K Flip-Flops with Clear and Complementary Outputs

General Description

This device contains two independent negative-edge-triggered J-K flip-flops with complementary outputs. The J and K data is processed by the flip-flops on the falling edge of the clock pulse. The clock triggering occurs at a voltage level and is not directly related to the transition time of the negative going edge of the clock pulse. The data on the J

and K inputs may change while the clock is high or low without affecting the outputs as long as setup and hold times are not violated. A low logic level on the clear input will reset the outputs regardless of the logic levels of the other inputs.

Connection Diagram



TL/F/6367-1

Order Number DM54LS107AJ, DM54LS107AW, DM74LS107AM or DM74LS107AN
See NS Package Number J14A, M14A, N14A or W14B

Function Table

| Inputs | | | | Outputs | |
|--------|-----|---|---|---------|-------------|
| CLR | CLK | J | K | Q | \bar{Q} |
| L | X | X | X | L | H |
| H | ↓ | L | L | Q_0 | \bar{Q}_0 |
| H | ↓ | H | L | H | L |
| H | ↓ | L | H | L | H |
| H | ↓ | H | H | Toggle | |
| H | H | X | X | Q_0 | \bar{Q}_0 |

H = High Logic Level

X = Either Low or High Logic Level

L = Low Logic Level

↓ = Negative going edge of pulse.

Q_0 = The output logic level before the indicated input conditions were established.

Toggle = Each output changes to the complement of its previous level on each falling edge of the clock pulse.

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