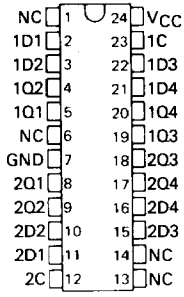
DECEMBER 1972 – REVISED DECEMBER 1983

- **Dependable Texas Instruments Quality and Reliability**

SN54100 . . . J OR W PACKAGE
SN74100 . . . J OR N PACKAGE
(TOP VIEW)



NC – No internal connection

description

These latches are ideally suited for use as temporary storage for binary information between processing units and input/output or indicator units. Information present at a data (D) input is transferred to the Q output when the enable (G) is high and the Q output will follow the data input as long as the enable remains high. When the enable goes low, the information (that was setup at the data input at the time the transition occurred) is retained at the Q output until the enable is permitted to go high.

These circuits are completely compatible with all popular TTL families. All inputs are diode-clamped to minimize transmission-line effects and simplify system design. Typical power dissipation is 40 milliwatts per latch.

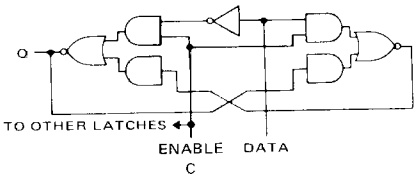
The SN54100 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN74100 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE
(Each Latch)

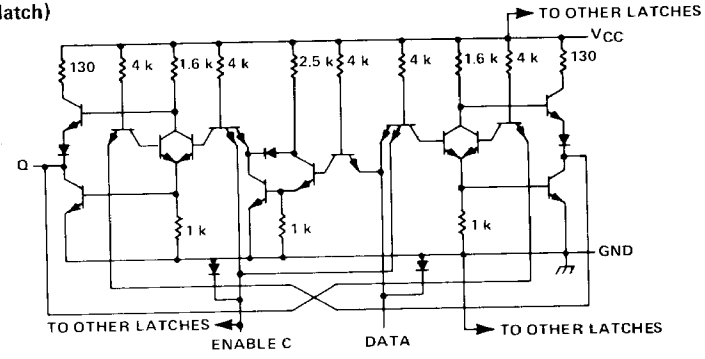
INPUTS		OUTPUTS	
D	G	Q	$\bar{Q}$
L	H	L	H
H	H	H	L
X	L	Q_0	$\bar{Q}_0$

H = high level, X = irrelevant
Q_0 = the level of Q before the high-to-low transition of G

logic diagram (each latch)



schematic (each latch)



Resistor values shown are nominal and in ohms.